REMARKS

Claims 1-17 remain in this application. Claim 1 has been amended. Applicants respectfully request reconsideration and review of the application in view of the foregoing amendments and following remarks.

Before addressing the merits of the rejections based on prior art, the following brief description of the invention is provided. The invention provides a DC-DC converter integrated in a land grid array (LGA) package. The DC-DC converter includes at least one vertically integrated power semiconductor die having a first electrode on a top surface and a second electrode on a bottom surface. In one embodiment, the package includes a substrate having multiple high density via arrays. Each high density via array is located directly beneath the power semiconductor die. In a preferred embodiment, each high density via array is electrically and thermally coupled to the power semiconductor die and an external pad of the LGA.

The Examiner rejected Claims 1-11 and 13-17 under 35 U.S.C. § 103(a) as unpatentable over Hashemi. This rejection is respectfully traversed.

Hashemi discloses a leadless flip-chip carrier structure. Flip-chip refers to a surface mount technology in which the semiconductor die is flipped over so that the active surface of the die faces the carrier. Electrical contact between the die and the carrier is achieved using solder bumps placed on the active surface of the die. The carrier comprises a substrate having support pads that engage the solder bumps of the flip-chip die. Underfill is dispensed in the interface area between the active surface of the die and the top surface of the substrate. This is because the solder bumps will change shape during the reflow process, and the underfill is necessary to maintain spacing between the die and the substrate. The substrate is provided with vias to provide an electrical connection through the substrate to a circuit board to which the carrier structure is attached.

In contrast, the present invention includes a semiconductor die having electrodes located on opposite surfaces. Hashemi discloses a semiconductor die having electrical

contacts only on the active surface—not on both surfaces. The invention does not utilize flip-chip technology, and thereby avoids the use of underfill. Moreover, the present invention includes a DC-DC converter circuit provided on the substrate, thereby providing an entire DC-DC converter module within a land grid array package. Hashemi fails to disclose a DC-DC converter circuit, and merely discloses a package carrying a single semiconductor die. Specifically, Hashemi fails to suggest or disclose, *inter alia*, a "DC-DC converter including at least one power silicon die having a top electrode surface and a bottom electrode surface, said bottom electrode surface being coupled to said die attach pad," as defined in Claim 1. This ground of rejection should therefore be withdrawn.

The Examiner rejected Claim 12 under 35 U.S.C. § 103(a) as unpatentable over Hashemi in view of Craft. This rejection is respectfully traversed.

Craft discloses an electronic circuit assembly having heat dissipating capabilities. The Examiner cites Craft merely for the disclosure of passive components within the circuit assembly. The reference otherwise fails to make up for the deficiencies of Hashemi discussed above. This ground of rejection should also be withdrawn.

In view of the foregoing, the Applicants respectfully submit that Claims 1-17 are in condition for allowance. Reconsideration and withdrawal of the rejections is respectfully requested, and a timely Notice of Allowability is solicited. To the extent it would be helpful to placing this application in condition for allowance, the Applicants encourage the Examiner to contact the undersigned counsel and conduct a telephonic interview.

While the Applicants believe that no fees are due in connection with the filing of this paper, the Commissioner is authorized to charge any shortage in the fees, including extension of time fees, to Deposit Account No. 50-0639.

Respectfully submitted,

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